Chhattisgarh Swami Vivekananda Technical University, Bhilai

Semester: B.Tech – 3rd **Branch: All branches**
Subject: Mathematics- III **Course Code: B000312(014)**

Total Marks in End Semester Exam: 100 **L: 3 T: 1 P: 0 Credits 4**
Minimum number of Class Tests: 02

Course Objectives:

1. To provide knowledge of Laplace transform of elementary functions including its properties and applications to solve ordinary differential equations.
2. To have thorough knowledge of partial differential equations which arise in mathematical descriptions of situations in engineering.
3. To study about a quantity that may take any of a given range of values that can't be predicted as it is but can be described in terms of their probability.
4. To provide a thorough understanding of interpolation and methods to solve ordinary differential equation.

UNIT-I Laplace transform: Definition, Transform of elementary functions, Properties of Laplace transform, Transform of derivatives & integrals, Multiplication by t^n, Division by t, Evaluation of integrals, Inverse Laplace Transform, Convolution theorem, Unit step function, Unit impulse function, Periodic function, Application to solution of ordinary differential equations.

UNIT- II Partial differential equation: Formation, Solution by direct integration method, Linear equation of first order, Homogeneous linear equation with constant coefficients, Non-homogeneous linear equations, Method of separation of variables.

UNIT- III Random variable: Discrete and continuous probability distributions, Mathematical expectation, Mean and Variance, Moments, Moment generating function, probability distribution, Binomial, Poisson and Normal distributions.

UNIT- IV Interpolation with equal and unequal intervals: Finite differences, Newton's Forward & Backward Difference Formulae, Central Difference Formula, Stirling's Formula, Bessel's Formula, Lagrange's Formula and Newton's Divided Difference Formula.

UNIT-V Numerical Solution of Ordinary Differential Equations: Picard's Method, Taylor's Series Method, Euler's Method, Euler's Modified Method, Runge-Kutta Methods, Predictor-corrector Methods- Milne's Method, Adams-Bashforth Method.

Text Books:

1. "Higher Engg. Mathematics", Dr. B.S. Grewal– Khanna Publishers.
2. "Advanced Engg. Mathematics" , Erwin Kreyszig – John Wiley & Sons.
3. "Numerical Methods in Engineering and Science" , Dr. B.S. Grewal, Khanna Publishers.
4. "Numerical Methods for Scientific and Engineering Computation" , M .K. Jain, S. R. K

Reference Books:

1. "Applied Mathematics", P. N. Wartikar& J. N. Wartikar. Vol-II Pune Vidyarthi Griha Prakashan, Pune.
2. "Applied Mathematics for Engineers & Physicists", Louis A. Pipes- TMH.
3. "Numerical Methods for Scientists and Engineers" K. Shankar Rao, Prentice Hall of India.
4. "Numerical Methods" P. Kandasamy, K. Thilagavathy and K. Gunavathi, S. Chand publication.

Course outcomes: After studying the contents of the syllabus in detail the students will be able to: Define (mathematically) unit step unit impulse, Laplace transform its properties, inverse and applications to solve ordinary differential equations and find Numerical solution of differential equations, which may be arising due to mathematical modelling based on engineering problems. Hands on these Mathematical topics will make them equipped to prepare for higher studies through competitive examinations.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Branch: Electronics & Telecommunication

Semester: III

Subject: **Electronic Devices** Code: **B000311(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100
Minimum Marks: 35

Course Objectives:

1. To study semiconductor charge carriers transport phenomena.
2. To understand practical applications of PN junction diode.
3. To understand the basic working physics of BJT and study transistor biasing arrangements.
4. To study basic principle of JFET, MOSFET their characteristics and amplifiers.

UNIT- I: Conduction in Semiconductor: Transport phenomena in semiconductors: Mobility and conductivity, Electrons and holes in an intrinsic semiconductor, Donor and acceptor impurities, Charge densities in a semiconductor, Law of mass action, Charge neutrality equation, Generation and recombination of charge carriers, Diffusion, Continuity equation, Injected minority carrier, Potential variation in a graded junction. Formation of p-n junction and its characteristics.

UNIT-II: Diode and its Application: Semiconductor Diode: Construction, current components, V-I Characteristics, Effect of Temperature on V-I Characteristics, Ideal Diode, Diode equation, Diode Resistance, Diode Capacitance: Transition and Diffusion Capacitance. Load line analysis of diode circuit, DC analysis of diode circuits: Piecewise linear model of p-n junction diode.
Rectifiers: Half wave, Full wave and Bridge rectifier: Voltage regulation, Ripple factor, Ratio of rectification, PIV, Transformer Utilization factor. Filter circuits for power supply(Qualitative analysis only): Inductor filter, Capacitor filter, CLC or π filter.
Zener diode: Break down mechanism, Characteristics, Specifications, Voltage regulator circuit using zener diode.

UNIT-III: Bipolar Junction Transistor & Its Configurations: Introduction, Construction, Types: npn and pnp, Current components. Transistor as an amplifier, Transistor Characteristics (input, output and transfer), Transistor Circuit Configuration: CB, CC, CE Configuration, Early Effect. Ebers-Moll Model. Transistor as a Switch.
Transistor biasing & Thermal stabilization: Concept of operating point, Thermal runway, Bias stability, Stability factors, Fixed bias, Collector to base bias, Voltage divider bias.

UNIT-IV: Junction Field Effect Transistor(JFET): JFET Construction, Symbol, Basic Operation, V-I Characteristics, Cut-off and pinch off voltages, Trans-conductance, CS, CG and CD Configuration, FET as switch, FET as VVR.
Biasing arrangements for JFET: Fixed bias, Self bias and Voltage divider bias.

UNIT-V: Metal Oxide Semiconductor Field Effect Transistor (MOSFET): Introduction, Construction, Symbol, Basic Operation, V-I Characteristics. MOSFET Types: Depletion MOSFET, Enhancement MOSFET, their characteristics and parameters, Body effect, Sub threshold conduction, The MOS Switch, CMOS devices. **MOSFET Biasing:** Fixed bias, Self bias and Voltage divider bias, Feedback bias in E-MOSFET.

Text Books:

1. Integrated Electronics: Analog & Digital Circuit Systems – Jacob Millman & Halkias, Tata McGraw Hill. (Unit- I, II & III)
2. Principles of Electronics by V. K. Mehta, Khanna Publication.
3. Electronic Devices and Circuit Theory – Robert L. Boylestad & L. Nashelsky, K.. L. Kishore, 9th Edition, PHI. (Unit- IV, V)
4. Electronic Devices & Circuits – Donald A Neaman, Tata McGraw Hill.

Reference Books:

1. *Electronic Devices & Circuits – Allen Mottershead, PHI.*
2. *Microelectronic Circuits - Sedra and Smith, 5th Edition, Oxford University Press.*

Course outcomes:

At the end of this course students will demonstrate the ability to

1. Understand the principles of semiconductor Physics
2. Understand and utilize the mathematical models of semiconductor junctions and MOS transistors for circuits and systems.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Branch: Electronics & Telecommunication

Semester: III

Subject: **Digital System Design** Code: **B000313(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)

ESE Duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

1. To Design, Analyze and Interpret Combinational Circuits
2. To Design, Analyze and Interpret Sequential Circuits

UNIT- I: Boolean Algebra & Minimization Techniques: Logic Simplification and Combinational Logic Design, ***Boolean Algebra:*** Logic Operations; Axioms and Laws of Boolean Algebra: Complementation Laws, AND Laws, OR Laws, Commutative Laws, Associative Laws, Distributive Laws, Absorption Laws, Transposition Theorem, De Morgan's Theorem; Duality; Reducing Boolean Expressions; Functionally Complete Sets of Operations; Boolean Functions and their Representation. ***Minimization Techniques***: Expansion of a Boolean expression to SOP form; Expansion of a Boolean expression to POS form; Karnaugh maps up to 4 variables, Mapping and minimization of SOP and POS expressions; Concept of Don't Care Terms; Quine – McClusky Method (Up to 5 variable); Synthesis using AND-OR, NAND-NOR and XOR forms; Design Examples; Binary codes and code conversion(BCD, Excess-3, Gray code)

UNIT-II: Combinational Circuits: MSI devices like ***Adder & Subtractor***: Half and Full Adders, Half and Full Subtractor, Serial and Parallel Adders, BCD Adder, ***Comparators***, ***Decoder:*** 3-Line to 8-Line Decoder, 8-4-2-1 BCD to Decimal Decoder, BCD to Seven Segment

Decoder; ***Encoder:*** Octal to Binary and Decimal to BCD Encoder; ***Multiplexers:*** 2- Input Multiplexer,4-Input Multiplexer,16-Input Multiplexer; ***Demultiplexers***: 1-Line to 4-Line & 1-Line to 8- Line Demultiplexer; Applications of Multiplexers.

UNIT- III: Sequential Circuits: Building blocks of ***Flip-Flops*** like S-R latch , Gated S-R Latch; D Latch, ***Edge Triggered Flip-Flops***: S-R, D, J-K and T Flips-Flops; Master-Slave J-K Flip-Flop; ***Shift registers:*** SISO, SIPO, PISO,PIPO, Bi-Directional Shift Registers, Universal Shift register; ***Counters:*** Asynchronous Counters: Design of Asynchronous Counters; Ripple Counters: Effects of Propagation Delay in Ripple Counters; Synchronous Counters: Design of

Synchronous Counters, 3-bit Synchronous Up counter, 3-bit Synchronous Down Counter,3-bit Synchronous Up-down Counter, Design Of Synchronous BCD Counter.

UNIT-IV: Finite State Machine: Design of synchronous Finite state machine, Algorithmic State Machines charts. Designing synchronous circuits like Pulse train generator, Pseudo Random Binary Sequence generator, Clock generation.

UNIT-V Digital Logic Families: Introduction; Logic Families: TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out, Tristate TTL, TTL subfamilies : IIL, ECL, MOS Logic, CMOS Logic, Comparison Among Various Logic Families, Manufacturer's Specification.

Text/Reference Books:

1. R.P. Jain, "Modern digital Electronics", Tata McGraw Hill, 4th edition, 2009.
2. W.H. Gothmann, "Digital Electronics- An introduction to theory and practice", PHI, 2nd Edition ,2006.
3. D.V. Hall, "Digital Circuits and Systems", Tata McGraw Hill, 1989
4. Digital Fundamentals: Floyd & Jain: Pearson Education.
5. Digital Electronics: A. P. Malvino: Tata McGraw Hill.

Course outcomes:

At the end of this course students will demonstrate the ability to

1. Employ Boolean algebra and circuit minimization techniques.

2. Design and analyze combinational logic circuits such as adders, subtractors, multiplexers, flip-flops, shift registers and counters.

3. Design & analyze modular combinational circuits with MUX/DEMUX, Decoder,

Encoder

4. Design & analyze synchronous sequential logic circuits

5. Gain knowledge about various logic families and select a suitable one for a specific application.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Branch: Electronics & Telecommunication
Semester: III

Subject: **Network Theory** Code: **B000314(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE Duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

- To understand the basic concepts and analysis of electric circuits.
- T o make the students learn how to synthesize an electrical network from a given impedance / admittance function.

UNIT-I:Methods of Analysing Circuits & Network Theorems: Node and Mesh Analysis, Source transformation and duality. Network theorems: Superposition, Reciprocity,Thevenin's, Norton's, Maximum power Transfer, Compensation and Tellegen's theorem as applied to AC circuits.
Input Power and Power Transfer: Energy and Power, Effective or Root- Mean Square Values, Average Power and Complex Power, Problems in Optimizing Power Transfer.

UNIT-II: Initial Conditions in Networks: Initial Conditions in Elements, Geometrical Interpretation of Derivatives, A Procedure for Evaluating Initial Conditions, Initial State of a Network.

UNIT-III: The Laplace Transformation :Introduction,TheLaplace Transformation, Basic Theorems for the LaplaceTransformation, Convolution Theorem, Application of Laplace Transformation Technique in Electric Circuit Analysis.
Transforms of Signal Waveforms: The Shifted Unit Step Function, The Ramp and Impulse Functions, WaveformSynthesis, The Initial and Final Value of f(t) from F(s).

UNIT-IV: Two Port Networks: Relationship of Two-Port Variables, Short-circuit Admittance Parameters, The Open CircuitImpedance Parameters, Transmission Parameters, The Hybrid Parameters, Relationships between Parameters Sets, Interconnection of Two-Port Networks: Series, Parallel and Cascade connection.

UNIT-V: Sinusoidal Steady State Analysis: The Sinusoidal Steady State, The Sinusoid and $e^{\pm j\omega t}$; Solution Using $e\pm j\omega t$;Solution Using $Re^{j\omega t}$ or $Ime^{j\omega t}$; Phasors and Phasor Diagrams.

Text/Reference Books

1. Van, Valkenburg.; "Network analysis"; Prentice hall of India, 2000
2. Sudhakar, A., Shyammohan, S. P.; "Circuits and Network"; Tata McGraw-Hill New Delhi,1994
3. A William Hayt, "Engineering Circuit Analysis" 8th Edition, McGraw-Hill Education

Course Outcomes:
At the end of this course students will demonstrate the ability to

1. Understand basics electrical circuits with nodal and mesh analysis.
2. Appreciate electrical network theorems.
3. Apply Laplace Transform for steady state and transient analysis.
4. Determine different network functions.
5. Appreciate the frequency domain techniques.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Branch: Electronics & Telecommunication

Semester: III

Subject: **Data Structure using C++** Code: **B000315(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)

ESE Duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

1. To impart the basic concepts of data structures and algorithms.
2. To understand concepts about searching and sorting techniques
3. To understand basic concepts about stacks, queues, lists, trees and graphs.
4. To enable them to write algorithms for solving problems with the help of fundamental data structures

UNIT I: Principles of Object Oriented Programming: Basic Concepts of Object Oriented Programming, Benefits of OOPs, Classes and Objects: C Structures Revisited, Specifying a Class, Defining Member Functions, Making an Outside Function Inline, Nesting of Member Functions, Private Member Functions, Arrays Within a Class, Memory Allocation for Objects, Static Data M embers, Static Member Functions, Arrays of Objects, Objects as Function Arguments, Friendly Functions, Returning Objects. Constructors and Destructors: Constructors, Parameterized Constructors, Multiple Constructors in a Class, Constructors with Default Arguments, Dynamic Initialization of Objects, Copy Constructor, Destructors.

UNIT II: Operator Overloading and Inheritance: Defining Operator Overloading, Overloading Unary Operators, Overloading Binary Operators, Overloading Binary Operators Using Friends, Manipulation of Strings Using Operators, Rules for Overloading Operators, Function Overloading, Defining Derived Classes, Single Inheritance, Making a Private Member Inheritable, Multilevel Inheritance, Multiple Inheritance, Hierarchical inheritance, Virtual Base Classes, Abstract Classes.

UNIT III: Pointers and Runtime Binding: Pointers and their Binding, Address Operator &, Pointer Variables, Void Pointers, Pointer Arithmetic, Runtime Memory Management, Pointers to Pointers, This Pointer, Introduction to Virtual Functions, Need for Virtual Functions, Pointer to Derived Class Objects, Definition of Virtual Functions, Array of Pointers to Base Class Objects, Pure Virtual Functions, Abstract Classes

UNIT IV: Introduction to the data structures: Searching, Types of searching: Linear Search , Binary Search, **Sorting** ,Types of Sorting : Insertion Sort, Bubble Sort and Selection Sort.

Introduction to the Stack and Queue, Types of Queue : Simple Queue, Circular Queue and Priority Queue.

UNIT V: Linked List, Tree and Graphs: Introduction to the Linked List. **Trees:** Introduction, Different Types of Tree: Binary Tree, Binary Search Tree, Tree Traversal, AVL Tree. **Graph:** Graph Theory Terminology, Sequential Representation of Graphs, Graph Traversal.

Text Books:

1. Object oriented Programming with C++, E Balaguruswamy, 3rd Edition, Mcgraw-Hill .(Unit I, II & V)

2. Mastering C++, K.R.Venugopal, Raj Kumar and T.Ravi Shankar , Mcgraw-Hill. (Unit III)

3. Theory and Problems of Data Structures, Seymour Lipschutz, Schaum's Outline Series. (Unit IV)

Reference Books:

1. **C++ Complete Reference, H. Schildt , Mcgraw-Hill.**
2. **Object Oriented Programming in Turbo C++, Robert Lafore, Galgotia Pub.**
3. **C++ Primer plus, Stephen Prata, Galgotia Pub**
4. **The C++ Programming Language, Bjarne Stroustrup, Pearson**

Course Outcome:

1. For a given algorithm student will able to analyze the algorithms to determine the time and computation complexity and justify the correctness.
2. For a given Search problem (Linear Search and Binary Search) student will able to implement it.
3. For a given problem of Stacks, Queues and linked list student will able to implement it and analyze the same to determine the time and computation complexity.
4. Student will able to write an algorithm Selection Sort, Bubble Sort, Insertion Sort,
5. Quick Sort, Merge Sort, Heap Sort and compare their performance in term of Space and Time complexity.
6. Student will able to implement Graph search and traversal algorithms and determine the time and computation complexity.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Name of program: Bachelor of Technology

Branch: Electronics & Telecommunication

Semester: III

Subject: **Electronic Devices Laboratory** Code: **B000321(028)**
Total Lab Periods: 36 Batch Size: 20
Maximum Marks: 40 Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To draw the characteristics of a semiconductor p-n junction diode and to find cut-in voltage, reverse resistance, static resistance and dynamic resistance.

2. To simulate characteristics of pn junction using SPICE model.

3. To draw the characteristics of a zener diode and to find cut-in voltage, reverse resistance, static resistance and dynamic resistance.

4. To design a half wave rectifier and to determine its efficiency and ripple factor.

5. To design a centre tap full wave rectifier and determine the ripple factor and efficiency with and without filter.

6. To design a bridge full wave rectifier and determine the ripple factor and efficiency with and without filter.

7. To draw the characteristics of CE configuration of a transistor amplifier.

8. To draw the characteristics of CB configuration of a transistor amplifier.

9. To draw the characteristics of CC configuration of a transistor amplifier.

10. To simulate characteristics of BJT using SPICE model.

11. To design a Zener regulator circuit and to find the regulation characteristics.

12. To draw the load line and find Q-point of a transistor amplifier under CE configuration.

13. To design and verify the self bias circuit operation.

14. To design and verify the voltage divider biasing circuit.

15. To draw the characteristics of FET.

16. To simulate characteristics of FET using SPICE model.

17. To draw the characteristics of MOSFET.

Equipment/Machines/Instruments/Tools/Software Required:

Circuit components, Breadboard, Hook-up wire, Power supply, CRO, Function generator, Any simulation software –Package like SPICE or MATLAB.

Recommended Books:

1. Laboratory Manual for Electronic Devices and Circuits, 4th Ed., David A. Bell, PHI

2. Lab Manual of Electronic Devices by Paul B Zbar.

3. Microelectronics' An integrated approach' by Roger T. howe and Charles G. Sodini.

4. Electronic Devices Systems and Applications by Robert Diffenderfer, Cengage learning.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Name of program: Bachelor of Technology

Branch: Electronics & Telecommunication

Semester: III

Subject: **Digital System Design Laboratory** Code: **B000322(028)**
Total Lab Periods: 36 Batch Size: 20
Maximum Marks: 40 Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To Verify The Properties of NOR & NAND Gates As Universal Building Block.

2. Realization of Boolean Expression Using NAND Or NOR Gates.

3. To design and implement an X- OR Gate Using Only NAND Or NOR Gates Only.

4. To design and implement a Half Adder Circuit using Logic Gates And Verify its Truth table.

5. To design and implement a Full Adder Circuit And Verify its truth table (Using Two X-OR And 3 NAND Gates).

6. To design and implement a Half Subtractor Circuit by Using Basic Gates And Verify its truth table.

7. To design and implement a Full Subtractor Circuit by Using Basic Gates And Verify its truth table.

8. To design and implement a Circuit of 4 -Bit Parity Generator and Checker & Verify its truth table.

9. To design and implement a 4x1 Multiplexer using Logic Gates And Verify its truth table.

10. To design and implement a 1x4 De-Multiplexer using Logic Gates And Verify its truth table.

11. To design and implement a Programmable Inverter Using X-OR Gates & Verify its truth table.

12. To design Octal to Binary Encoder using Logic Gates and Verify its truth table.

13. To design BCD to Excess-3 Decoder using Logic Gates And Verify its truth table.

14. To design Binary to Gray Code Converter and Verify its truth table.

15. To Design A Comparator Circuit & Verify its truth table.

16. To Construct A RS Flip Flop Using Basic & Universal Gates (NOT, NOR & NAND)

17. To Construct A J.K. Master Slave Flip Flop & Verify its truth table

18. To Verify The Operation of A Clocked S-R Flip Flop And J. K. Flip Flop

19. To Construct A T & D Flip Flop Using J. K. Flip Flop And Verify Its Operations & truth table.

20. To Construct and study the operation of a 4-bit Shift Register in following modes:

    a. Serial In Serial Out

    b. Serial In Parallel Out

    c. Parallel In Serial Out

    d. Parallel In Parallel Out

21. To Verify the Operation of 4-bit Binary Asynchronous Counter.

22. To Verify The Operation of a Synchronous Decade Counter.

23. To perform the operation of BCD Counter Using 7490.

Equipment/Machines/Instruments/Tools/Software Required:

Various ICs , Power Supply, Hook-Up Wires.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Branch: Electronics & Telecommunication

Semester: III

Subject: **Electronics Workshop Laboratory** Code: **B000323(028)**
Total Lab Periods: 36 Batch Size: 20
Maximum Marks: 40 Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To understand the operational features of Analog and Digital Multimeter.

2. To understand the operational features of Cathode Ray Oscilloscope.(Calibration, Time/div, Volt/div, X-Y, single channel, Dual channel)

3. To understand the operational features of Function Generator (Measurement of volt and frequency, attenuation).

4. Measurement of capacitors (mica, ceramic, paper, electrolytic and variable) using CRO and LCR Meter and verify with color coding.

5. Measurement of resistors- Fixed (carbon, wire wound, metal film and variable) using CRO and Multimeter and verify with color coding and identification of special resistors like Thermistor, LDR and VDR (FET)

6. Measurement of inductors (fixed) using CRO and LCR meter.

7. Study of Diodes (Ge and Si), Zener diodes and LEDs.(terminals, resistance and capacitance in forward biased and reversed biased conditions).

8. Study of Transistors (npn, pnp) using multimeter and CRO. (terminals, forward biased and reversed biased junction conditions.)

9. To understand the types of PCB.

10. To understand PCB designing rules (Art Work and layout) using EDA tools.

11. To design and fabricate a DC power supply using bridge rectifier on PCB.

12. To learn the use of SMD rework station.

13. Mini project (compulsory)

Equipment/Machines/Instruments/Tools/Software Required:

- Film Making unit
- Deep coating machine
- UV exposure unit
- PCB curing machine
- PCB etching machine
- PCB drilling machine
- PCB tining machine
- Magnifying lamp
- Soldering &desoldering iron
- LCRQ meter
- Digital & analog multimeter
- PCB making software (ULTIBOARD, PROTEL, EXPRESS LAB, EDWin XP)
- Resistance color code chart
- Capacitor color code chart
- Transistor chart
- CRO.
- SMD work station

Recommended books:

1. A Monograph on Electronic design Principles – by N.C. Goyal& R.K. Khetan

2. Electronic Measurement and Instrumentation – by A.K. Shawney.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Name of program: Bachelor of Technology

Branch: Electronics & Telecommunication

Semester: III

Subject: **Software Laboratory** Code: **B000324(028)**
Total Lab Periods: 36 Batch Size: 20
Maximum Marks: 40 Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. A book shop maintains the inventory of books that one being sold at the shop. He list includes details such as authors, title, price, publisher and stock position. Whenever a customer wants a book, the sales person input the title and author and the system searches the list and displays whether it is available or not. If it is not, an appropriate message is displayed. If it is then the system displays the book details and requests for the number of copies required.

2. Write a program which will show the order of execution of constructor, destructor, static data member, static function and member functions.

3. Create class Distance having private data feet(type integer), inches(type float) and function getdist() and showdist() . Overload + operator to add two distance values and > operator to compare them.

4. Create a class called employee containing protected data name(20 characters), employee number(long integer). Also write its constructor and destructor functions. Create two derived classes called hourly _employee containing private data rate and hours and salary_ employee containing basic salary and allowances as data members. The class employee is inherited as public by these derived classes. Write appropriate functions in each class to calculate total salary of each employee and to display name, number and total salary.

5. Create a class dimension containing three float type data and a constructor to accept values, also declare a pure virtual function area() in it. Now create three derived classes rectangle, square and triangle, each inheriting dimension as public.Define corresponding constructors and redefine

virtual function area() in each to give area of respective figure. A main() program should create suitable objects to implement this inheritance.

6. Create a class STRING that contains a character array as a data member. Overload + and = operators respectively to concatenate and compare strings.

7. Create two classes DM and DB respectively represent the distance in meters, centimeters and distance in feet, inches. Write a program that can read values for the class objects and add one object DM with another object of DB. Use a friend function to carry out the addition operation. The object that stores the results may be a DM object or DB object depending on the units in which the results are required. The display should be in the format of feet and inches or meters and centimeters depending on the object on display.

8. Write a program to read the contents of a text file and count the number of words present in the file.

9. Write a program that reads a text file and creates another file that is identical except that every sequence of consecutive blank spaces is replaced by single space.

10. Write a program that will ask the users to enter the details of 5 students and transfer those details into a binary file Stud.dat. Write another file that will read the details of the students and print the names of all those students who have total marks greater that a particular given value.

11. Write a program that will take the details of 10 employees as input and transfer those details into a binary file. Write another program that will provide a menu to the user for the following purpose.

a. To sort the file on the basis of their employment number.
b. To sort the file on the basis of their name.
c. To search the record for a particular employee on the basis of their employee number or name.

12. Write a program that will take two strings from the command line as argument and print the appropriate message if both the strings are same.

13. Write a program to implement a stack and it's operations.

14. Write a program to implement a linear queue, circular queue using an array.

15. Write a program to convert an infix expression into its equivalent postfix expression using a stack.

16. Write a program to evaluate a postfix expression using a stack.

17. Write a program to create and display a linked list of integers.

18. Write a program to create a linked list and define functions to add a node (at the beginning, end and middle), delete a node, search a node and display all the nodes.

19. Write a program to create two linked list and append one list at the end of another using function.